Amendment to the Claims:

1. (Original) A device for controlling decoder extension cards and universal extension cards, comprising a receiver, a card reader, a control circuit, a processor, and a select circuit, characterized in that the receiver is connected, via the control circuit, with the processor, the select circuit and the card reader connected with a power supply circuit, and a first buffer, a second buffer and a third buffer are connected to the card reader, wherein the card reader is connected via the first buffer and the second buffer with the processor, and via the third buffer with the control circuit.

2. (Currently amended) A device according to claim 1, characterized in that, the select circuit comprises a first input ~~terminal~~, a second input ~~terminal~~, a third input ~~terminal~~ and a fourth input ~~terminal~~, a first multiplexer, a second multiplexer, a first inverter, a second inverter, a third inverter, a first NAND element and a second NAND element, wherein each of the first and third ~~input terminals~~ inputs of the control signal is connected with an input of one of the first and second multiplexers, while each of the first, second and fourth ~~input terminals~~ inputs of control signals is linked with an input of one of the first, second and third inverters, while an output of each of the first, second and third inverters is linked with one of the first and second NAND elements, and an output of each of the first and second NAND elements is linked to an input of one of the first and second multiplexers, and the first and second multiplexers are controlled by a signal generated by the processor.

3. (Original) A device for controlling decoder extension cards and universal extension cards incorporating a control circuit and a processor, characterized in that the device comprises a first card reader with a first power supply circuit, a second card reader with a second power supply circuit, a processor which is linked with the control circuit, wherein the input of the control circuit is linked to a receiver, wherein the processor is connected with a first select circuit controlled by a first signal and with a second select circuit controlled by a second signal, and the processor is connected with the first card reader via a first buffer for the first card reader, and a second buffer for the first card reader, and the processor is

connected with the second card reader via a first buffer for the second card reader, and a second buffer for the second card reader, and wherein the control circuit is linked with the first card reader via a third buffer for the first card reader, and is linked with the second card reader via a third buffer for the second card reader.

4. (Currently amended) A device, according to claim 3, characterized in that, each of the first and second select circuits comprise a first input ~~terminal~~, a second input ~~terminal~~, a third input ~~terminal~~ and a fourth input ~~terminal~~, a first multiplexer, a second multiplexer, a first inverter, a second inverter, a third inverter, a first NAND element and a second NAND element, wherein each of the first and third ~~input terminals~~ inputs of control signals are connected with an input of one of the first and second multiplexers, while each of the first, second and fourth ~~input terminals~~ inputs of control signals is linked with an input of one of the first, second and third inverters, and an output of each of the first, second and third inverters is linked with one of the first and second NAND elements, and an output of each of the first and second NAND elements is linked to an input of one of the first and second multiplexers, and the first and second multiplexers are controlled by signals generated by the processor.